# SRS_P1_HSI

## Contents

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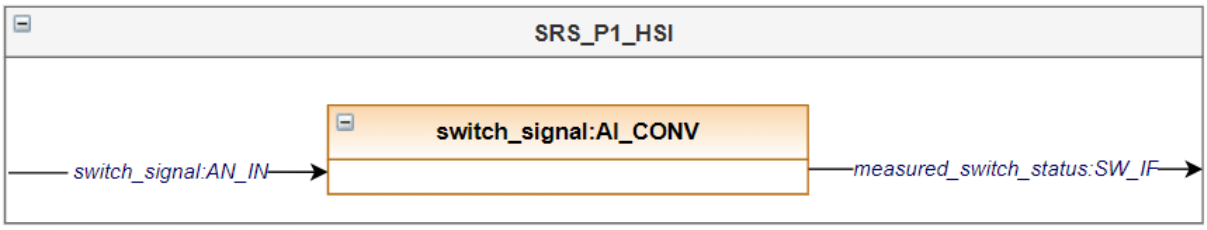
## 1 Scope

This doc is describing the HW – SW Interface.

## 2 Internal_Block_Diagram = its_IBD()

*(Note: This diagram is automatically generated out of information provided from the project specific RML classes)*



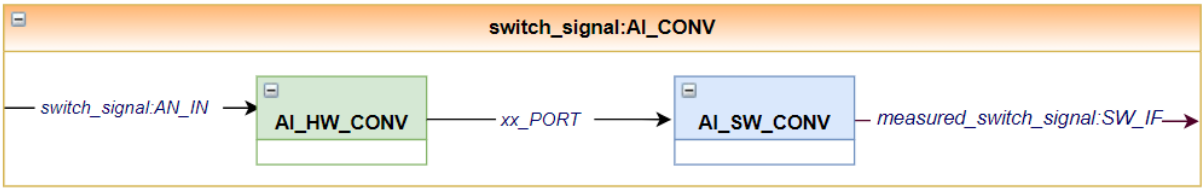

## 3 Funct_Req_dscr = switch_signal:AI_CONV

### 3.1 Scope

Conversion of analog signal into SW signal.

### 3.2 AI_CONV_Diagram = its_IBD()

*(Note: This diagram is automatically generated out of information provided from the project specific RML classes)*



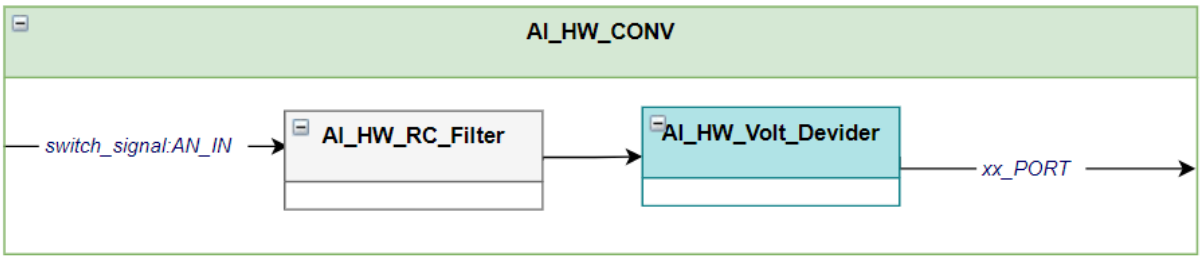

### 3.3 SubComponent = AI_HW_CONV

#### 3.3.1 Scope

HW-conversion of analog input signal

#### 3.3.2 HW_Conv_Diagram = its_IBD()

*(Note: This diagram is automatically generated out of information provided from the project specific RML classes)*



### 3.3.3 SubComponent1 = AI_HW_RC_Filter

Comp_Funct = Passive RC-Filter for noise reduction

**SRDH-908** - Its_power_supply = N/A

**SRDH-909** - PRTY_Filter_type = High Pass

**SRDH-811** - PRTY_3db_Filter_freq = 200 Hz

### 3.3.4 SubComponent2 = AI_HW_Volt_Devider

Comp_Funct = u_VoltDev_out =k * u_VoltDev_IN

Formula_k = R2 / (R1 plus R2)

**SRDH-832** - Its_power_supply = N/A

**SRDH-835** - PRTY_Transfer_factor_k = 4.7k/(12k+4.7k) = 0.281

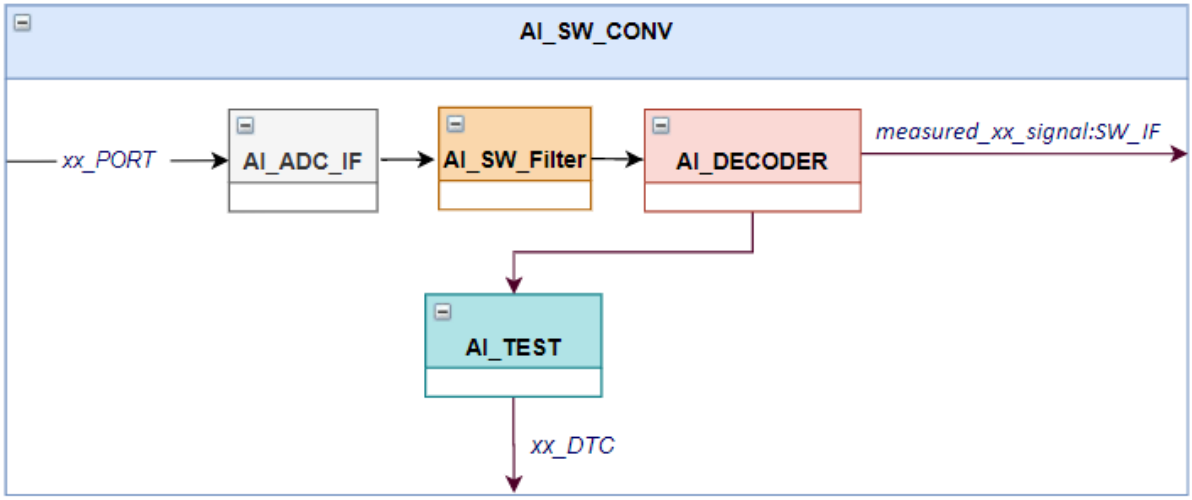
## 3.4 SubComponent = AI_SW_CONV

### 3.4.1 Scope

SW conversion reqs of analog input signals

### 3.4.2 SW_Conv_Diagram = its_IBD()

*(Note: This diagram is automatically generated out of information provided from the project specific RML classes)*




### 3.4.3 SubComponent1= AI_ADC_IF

Comp_Funct = Conversion of analog sigto digital sig.

**SRDH-895** - Port = tbd

*3.4.3.1 PRTY_ADC = ADC_Block_PRPTYs*

Scope = ADC Block Initializations

**SRDH-888 -** Sampling_Frequency = tbd

**SRDH-889 -** Sampling_Mode = tbd

**SRDH-890 -** AD_Resulution = tbd

**SRDH-891 -** Reference_Voltage = tbd

### 3.4.4 SubComponent2= AI_SW_Filter

Comp_Funct = FIFO-Buffer and Filter-Process

**SRDH-884 -** Execution_rate = tbd

**SRDH-885 -** PRTY_Buffer_Size = tbd

**SRDH-886 -** PRTY_Filter_Process = Averaging of ADC samples

### 3.4.5 SubComponent3 = AI_DECODER

Comp_Funct = Decoding of ADC values

**SRDH-873 -** Execution_rate = tbd

**SRDH-876 -** [1..*)xx_STATE = “xx V <= U < xxV”

**SRDH-875 -** Default_Value= tbd

### 3.4.6 SubComponent4 = AI_TEST

Comp_Funct = Test of decoded AI signal values

**SRDH-868 -** Execution_rate = tbd

*3.4.6.1 (0..*) PRTY_DTC_Handling = xx:DTC*

**SRDH-856 -** DTC_number = tbd

**SRDH-857 -** Err_Detect_Crit = tbd

**SRDH-858 -** DTC_Quali_Crit = tbd

**SRDH-859 -** DTC_Dequali_Crit = tbd

**SRDH-860 -** Error_Reaction = tbd

**SRDH-861 -** DTC_Indication = tbd

**SRDH-862 -** DTC_Delete_Protection = tbd

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## 4 Nonfunct_Req_descr = NF_Req

### 4.1 Quality_req

**SRDH-517 -** The system shall have high qualitiy

### 4.2 Reusability_req

**SRDH-516 -** All components of the system shall be reusable

### 4.3 Criticalty

**SRDH-515 -** Criticalty = tbd

## 5 Abbreviations = Used_Abbreviations

P1 = Project 1 (Example Project)
BCP = Body Control Platform
ECU = Electronic Control Unit
IF = Interface
SF = System Function
SRD = System Requirement Description
SUPL = Supplement
UC = Microcontroller
PLCC = Plastic Leaded Chip Carrier
NVM = Non-volatile memory
RAM = Random access memory
EEPROM = electrically erasable programmable read only memory
Dig_IO = Digital Input Output
ADC = Analog Digital covnerter
CAN = Controller Area Network
tbd = To be defined
PWM = pulse wide modulation
I2C = Inter-Integrated Circuit
SPI = Serial Peripheral Interface
UART = Universal Asynchronous Receiver Transmitter
init = initialization
req = requirement
NF_Req = non-functional requirement